EUROMICRO DSD 2026 - Conference Programme

Wednesday, September 2

Time	Room A	Room B	Room C
08:30-09:00	Welcome Session		
09:00-10:30	**Keynote 1 - Torvald Martensson (Saab AB and Linkoping University): Testing and Test Environments for Large-Scale Cyber-Physical Systems**		
10:30-11:00	Coffee Break		
11:00-12:30	**DSD 1-1 | Room A** **Edge AI: Efficient Inference and Adaptation** **Chair: TBD**	**DSD 1-2 | Room B** **Architectures and Hardware for Security Applications (AHSA), Part 1 of 2** **Chair: TBD**	**DSD 1-3 | Room C** **Opensource Methods, Architectures, Tools and Technologies for RISC-V (MATTERV)** **Chair: TBD**
	11:00-11:20 Zahra Kokhazad, Milad Kokhazadeh, Georgios Keramidas, Vasilios Kelefouras and Panagiotis Mousouliotis. "Adaptive Low-Rank Factorization for Dynamic DNN Inference on Edge Devices".	11:00-11:20 Youness Ayyada, Athanasios Papadimitriou, Stavros G. Stavrinides, Stefan Katzenbeisser, Tolga Arul and Nikolaos Athanasios Anagnostopoulos. "Assessment of LM35 Temperature Sensors for True Random Number Generation".	11:00-11:20 Joël Porquet-Lupine, Kushagra Tiwari and Shengmin Liu. "LupIO-RTL: A Lightweight and Open-Source I/O Device Suite for SoC Prototyping and Research".
	11:20-11:40 Erhon Aragão, André Wolff, Galeano Domingues, Dennis Balreira, Luigi Carro and Gabriel Nazar. "Exploiting Token Concentration for Energy-Efficient Embedding Caching in Edge AI".	11:20-11:40 František Dejm, David Pokorný, Petr Socha and Martin Novotný. "Detecting Program Cycles through Power Consumption".	11:20-11:40 Eslam Hussein, Bernd Waschneck and Christian Mayr. "Analytical-vs-Realized Gaps in RISC-V Custom Instruction Flows".
	11:40-12:00 Aravind Pradeep, Samira Nazari, Mahdi Taheri and Christian Herglotz. "Fusion: A Framework for Unified Sequential Token Adaptation in VisION Transformers".	11:40-12:00 Antonio Saavedra, Jan Caspar Marx, Lars Renkes and Jean-Pierre Seifert. "The Achilles' Heel of Partial Reconfiguration: Optical Side-Channel Leakage on the 7-Series ICAP".	11:40-12:00 Yilou Wang. "Enabling Industrial-Grade RISC-V UVM Verification on an Open-Source Simulator".
	12:00-12:20 Avik Bhatnagar, Federico Nicolás Peccia and Oliver Bringmann. "TASTE: Throughput-Aware Batch Size Tuning for On-Device Edge Learning".	12:00-12:20 David Pokorný, Petr Socha and Martin Novotný. "Vote-Based Attack on High-Order Share-Slicing Masking".	12:00-12:20 Tobias Scheipel. "On the Impact of Automated Testing and Real-time Feedback on Student Learning in RISC-V Digital Design Education: A Comparative Study".
	12:20-12:30 [WiP] Matthias Dippold, Sofia Maragkou, Grigorios Chrysos, Matthias Wess, Thilo Sauter and Sotiris Ioannidis. "A Dual-Head Model for Host based Intrusion Detection Systems on System-Call traces".	12:20-12:30 [WiP] Ludovic Claudepierre, Edna Rocio Ferrucho-Alvarez, Laurent Le Brizoual and Laurent Pichon. "Clock-glitch Fault Characterization by Timing Comparison with Laser Fault Injection".	12:20-12:30 [WiP] Jan Ber. "Design and implementation of three-stage RISC-V microprocessor for education".
12:30-14:00	Lunch Break		
14:00-15:30	**Keynote 2 - Andreas Eckel (TTTech Computertechnik AG): title to be announced**		
15:30-16:00	Coffee Break		

	DSD 2-1 | Room A **Hardware Accelerators for Neural Networks** **Chair: TBD**	**DSD 2-2 | Room B** **Real-Time Systems and Resource Management** **Chair: TBD**	**DSD 2-3 | Room C** **Hardware, Software, and Tools for the IoT-to-Edge-to-Cloud Continuum (HSTIEC)** **Chair: TBD**
16:00-17:30	16:00-16:20 Shashank S, Shravan Kumar Lekkala, Pranava M, Nipun Sagiraju, Devikarani H S and Madhav Rao. "Hardware-Efficient Fused Logarithmic Attention Unit with Mixed Base Softmax (MBS)".	16:00-16:20 Elena Mariolina Galdi, Filippo Muzzini, Nicola Capodieci, Paolo Burgio and Andrea Marongiu. "Improving Task-Set Execution on Embedded GPUs via Spatial Partitioning".	16:00-16:20 Bilel Tarchoun, Taha Yassine Abidi, Iyad Dayoub and Ihsen Alouani. "ApproxGuard: Defending Federated Learning Against Data Reconstruction via Approximate Computing".
	16:20-16:40 Suraj Karki, Qazi Arbab Ahmed and Thorsten Jungeblut. "No Attention, No Problem: DPU-Aware Attention Approximation in Modern YOLO on FPGA".	16:20-16:40 Davide Mor, Giovanni Agosta and Federico Terraneo. "EVA: A Rust-based Embedded Real-time Operating System with Kernel Memory Safety".	16:20-16:40 Shunsuke Ito and Takuya Azumi. "VAST: V2X/Dynamic Map-Aware Autonomous Driving Systems Validation Toolchain".
	16:40-17:00 Ertuğrul Keskin and Arda Yurdakul. "Memory-Efficient Spiking Neural Network Training with Backpropagation-Free Learning Rules".	16:40-17:00 Narimene Elhettak, Houssam-Eddine Zahaf and Khaoula Boukir. "Transparent GPU Partitioning and Scheduling for Concurrent Real-Time Kernels".	16:40-17:00 Federico Aromolo, Daniel Casini and Matthias Becker. "Counterexample-Guided Exploration of Real-Time Models with CBMC: A Weakly-Hard Case Study".
	17:00-17:20 Sneha Dandekar, Vaishnavi Sharma and Madhav Rao. "Posit-Based Mixed Precision Systolic Array For Neural Inference".	17:00-17:20 Jon Altonaga, Enrico Mezzetti, Irune Agirre, Jaume Abella and Francisco Cazorla. "Memory Bandwidth Regulation for Time-constrained Containerized Applications".	17:00-17:20 Mouad Zouhdi, Jiahe Guo, Rafik Hammadi, Binqi Sun, Philippe Leleux, Tomasz Kloda et al. "Pruning of Deep Neural Networks for Real-Time Execution on Edge TPU".
	17:20-17:30 [WiP] Federico Buccellato, Luca Mannini and Corrado De Sio. "A Compiler-Aware Framework for Partitioned Neural Network Inference on FPGA DPUs".	17:20-17:30 [WiP] Vadim Peczyński and Joanna Szłapczyńska. "Microservice Decomposition using Many-Objective Optimization".	17:20-17:30 [WiP] João Maia Aguiar and José Machado Da Silva. "A Low-Power ADC-Free Resistive Sensor Readout Circuit for uC-Based Microsystems".

Thursday, September 3

Time	Room A	Room B	Room C
09:00-10:30	**Keynote 3 - Davide Rossi (University of Bologna, Fondazione Chips-IT): Past, Present and Future of RISC-V - The PULP Perspective**		
10:30-11:00	Coffee Break		
	DSD 3-1 | Room A **In-Memory and Dataflow Computing** **Chair: TBD**	**DSD 3-2 | Room B** **Architectures and Hardware for Security Applications (AHSA), Part 2 of 2** **Chair: TBD**	**DSD 3-3 | Room C** **Design Automation and EDA Tools** **Chair: TBD**
	11:00-11:20 Pierre-Olivier Ankou, Anca Molnos, Kamel-Eddine Sadadou, Romain Lemaire, Jonathan Miquel, Guillaume Prenat et al. "Multi-Level VG-SOT In-Memory Computing for Embedded Transformer Inference".	11:00-11:20 Ali Ait Hassou, William Pensec, Florent Bruguier and Pascal Benoit. "TagGuard: Peripheral-to-Pipeline Hardware DIFT for Bare-Metal RISC-V".	11:00-11:20 Níkolas Padão Schuster and Gabriel Luca Nazar. "Expanding the FPGA HLS Design Space with Target Frequency Exploration".
11:00-12:30	11:20-11:40 Saeideh Nabipour, Saeideh Shirinzadeh and Rolf Drechsler. "A Design Automation Framework for Approximate MAGIC-Based Dadda Tree Multipliers in Memristive In-Memory Computing".	11:20-11:40 Marios Papadopoulos, Kostas Lampropoulos and Paris Kitsos. "An Efficient Keccak-based FPGA Architecture for 5G Authentication and Key Agreement Protocol".	11:20-11:40 Petr Bardonek and Marcela Zachariášová. "Static Analysis Driven Methodology for Automating Vertical Reuse of Portable Stimulus Models".

	11:40-12:00 Julius Wührer, Patrick Schmid, Alexander Richard Manfred Borst and Oliver Bringmann. "WindowBuffet: A Dataflow-Orchestrated Inter-Compute Buffer with Decoupled Memory Offloading for Multi-Accelerator Systems".	11:40-12:00 Francesco Antognazza, Enrico Manfredi, Valeria Piscopo, Alessandra Dolmeta, Mattia Mirigaldi, Guido Masera et al. "A Multi-Dimensional Design Space Exploration of ChaCha20 on FPGA".	11:40-12:00 Mohamed Soliman, Mohamed Gaber, Joonas Multanen, Tero Lehtinen and Pekka Jääskeläinen. "Open-Source Spatial-Aware Scan-Chain Optimizer for OpenROAD".
	12:00-12:10 [WiP] Federico Nicolás Peccia, Avik Bhatnagar and Oliver Bringmann. "Autotuned Distribution of Multi-DNN Workloads on Multi-Accelerator SoCs".	12:00-12:20 Severin Brunner and Sebastian Altmeyer. "A real-time AES hardware accelerator supporting simultaneous encryption requests".	12:00-12:20 Sumiran Mehra, Todor Stefanov and Nele Mentens. "FPGA-Diff: Differential Bitstream Mechanisms for Efficient Secure Remote Updates of FPGAs".
	12:10-12:20 [WiP] Nadeem Abbas and Nazia Shahzadi. "Large Language Models for Software Architecture Design Support in Self-Adaptive Systems: Early Insights from an Exploratory Systematic Review".	12:20-12:30 [WiP] Raphaël Wintersdorff, Renaud Pacalet and Laurent Sauvage. "Operation Count as a Performance Predictor: An Empirical Study of Lightweight AEAD Schemes".	12:20-12:30 [WiP] Norbert Fijałek, Ilona Bluemke and Piotr Gawrysiak. "Knowledge Retrieval Architectures for AI-Assisted Software Development: From Static Context to Autonomous Development Agents".
12:30-14:00	Lunch Break		
14:00-15:30	**Keynote 4 - Jaroslaw Krolewski (Synerise, AGH University of Krakow): Synerise Case Study - Engineering Teams That Ship a Billion Decisions a Day - Peopleware at Production Scale**		
15:30-16:00	Coffee Break		
16:00-17:30	**DSD 4-1 | Room A** **FPGA Application Accelerators** **Chair: TBD**	**DSD 4-2 | Room B** **RISC-V Acceleration** **Chair: TBD**	**DSD 4-3 | Room C** **Dependability, Testing and Fault Tolerance in Digital Systems (DTFT) and Digital Design and Verification with Chisel (DDVC)** **Chair: TBD**
	16:00-16:20 Zohaib Hassan, Aleksandr Ometov, Elena Simona Lohan and Jari Nurmi. "A Reconfigurable CGRA-Based Transmitter Architecture for Delay-Doppler Waveforms".	16:00-16:20 Or Avivi, Michal Sojka, Uffke Drechsler and Pavel Zaykov. "Accelerating SpMV for FP16 Block-Sparse Matrices on Embedded RISC-V Core via Custom Instructions".	16:00-16:20 Luca Müller, Mohamed Nadeem and Rolf Drechsler. "Scalability Matters: Future-Proof Formal Verification of a RISC-V Arithmetic Logic Unit".
	16:20-16:40 Felipe Winkler, Carolina Gallardo-Pavesi, Yaime Fernández, Javier E. Soto, Cecilia Hernández and Miguel Figueroa. "FPGA-Based Sliding-Window Quantile Estimation for High-Speed Network Traffic Measurement".	16:20-16:40 Grigorios Chaseropoulos, Angelos Athanasiadis, Nikolaos Tampouratzis and Ioannis Papaefstathiou. "Acceleration of BFV Homomorphic Encryption on RISC-V Vector CPUs".	16:20-16:40 Sabir Khanlarov and Petr Fišer. "Multiple-Vector Random Access Scan Test Compression Algorithm".
	16:40-17:00 Carolina Gallardo-Pavesi, Javier E. Soto, Joaquín Montero, Álvaro Guzmán, Gian Luca Barbagelata, Cecilia Hernández et al. "An FPGA Accelerator for Genomic Similarity Matrix Estimation Using SuperMinHash Sketches".	16:40-17:00 Arbi Gunbardhi. "A Fine-Grained Multithreaded RISC-V Core for Efficient and Predictable Real-Time Microcontrollers".	16:40-17:00 Félix Ridoux, Souheib Baarir, Jean-Marc Daveau and Philippe Roche. "Incremental Bit-Precise Formal Fault Injection for Hardware Robustness and Security Verification".
	17:00-17:20 Fatemeh Mehrafrooz, Roozbeh Siyadatzadeh, Nele Mentens and Todor Stefanov. "Importance-Aware Encryption for Secure Distributed CNN Inference at the Edge".	17:00-17:10 [WiP] Ahmet Zahit Can and Erkan Uslu. "Dolunay: Architectural Support for Independent Thread Scheduling in a RISC-V SIMT Accelerator".	17:00-17:20 Abdullah Allam, Maarten Boersma and Sergio Seminara. "Advanced IP Verification with Chisel and pyuvm".
	17:20-17:30 [WiP] Lukasz Drzensla, Sebastian Koryciak, Oleksandr Savchenko and Paweł Russek. "Study of PicoTDC Performance for FIT Detector Upgrade in ALICE Experiment at CERN".	17:10-17:20 [WiP] Joao Andre and Alexandre Ferreira. "Instruction Flow Amplifier: A Novel Architecture for In-Order Processor Front-End Optimization".	17:20-17:30 [WiP] Stefan Biffl. "SIAM DSL: Accessible Structured Text for Bridging the Architecture-Impact Gap in Cyber-Physical Production Systems".

Friday, September 4

Time	Room A	Room B	Room C
09:00-10:00	**Keynote 5 - Mira Mezini (TU Darmstadt): AI-assisted Programming: From Intelligent Code Completion to Foundation Models. A Twenty-Year Journey**		
10:00-10:30	Coffee Break		
10:30-12:00	**DSD 5-1 | Room A** **Perception, Robotics and Monitoring** **Chair: TBD**	**DSD 5-2 | Room B** **European and Major Multi-Partner Projects in Digital Systems Design (EMPDSD), Part 1 of 2** **Chair: TBD**	**DSD 5-3 | Room C** **Safety, Security and Privacy of Cyber-Physical Systems (SPCPS) and Advanced Systems for Health Wellness and Personal Monitoring (ASHWPA)** **Chair: TBD**
	10:30-10:50 Ammar Bouketta, Smail Niar, Hamza Ouarnoughi and Eva Mutuzo Brindle. "Cycle-Aware Autoencoder with Cross-Signal Consistency for Railway Door Anomaly Detection".	10:30-10:50 Julian Wälde, Markus Fritscher, Tim Henkes, Fabian Buschkowski, Milan Funck, Tuba Kiyan et al. "Multi-Partner Project: DI-Sign-HEP - An Open and Industrially Applicable Hardware-Security Module".	10:30-10:50 Alejandro Casado-Galán, Erica Tena-Sánchez, Francisco Eugenio Potestad Ordóñez and Antonio J. Acosta. "Detection of Electromagnetic Side Channel Attacks on FPGA-based Cryptohardware".
	10:50-11:10 Arthur Nathaniel Mwang'Onda, Lester Kalms and Diana Goehringer. "Burst-Aware Hardware/Software Co-Design for Real-Time Point Cloud Registration on FPGA-SoC".	10:50-11:10 Catalin Bogdan Ciobanu, Francesco Conti, Cairo Caplan, Holger Schmidt, Wolfgang Ecker, Rob Wullems et al. "Forging Robust Building Blocks for Next-Gen RISC-V Chips: Virtual Repository and IP Card".	10:50-11:10 Muzaffer Citir, Hiroki Nishikawa and Sangyoung Park. "Client and Training Data Selection for Computationally-Efficient Synchronized Federated Learning".
	11:10-11:30 Mohammad Hasan Rahmani, Carlos Tiana Gomez, Pieter De Clercq, Anil Kumar Chavali, Shannon van de Velde, Nico Huebel et al. "A Real-Time Sensor Pose Monitoring Framework via Integrated Perception and World Modeling".	11:10-11:30 Lilia Zaourar, Benoit Tain, Raphael Millet, Mohamed Benazouz, Ayoub Mouhagir, Chouki Aktouf et al. "SoC Planner: An Integrated Solution for Sustainability-Aware SoC Exploration and RTL Generation".	11:10-11:30 Floriaan Bulten, Yawar Rasheed, Arlene John, Vincenzo Stoico and Ghayoor Abbas Gillani. "Toward Energy-Efficient and Low-Power Arrhythmia Detection for Wearable Devices".
	11:30-11:50 Lu Jiang, Matthias Nickel and Diana Goehringer. "A Reconfigurable FPGA Framework for Near-Linear DAG Acceleration for Robotics".	11:30-11:50 Norbert Druml, Martin Ebetshuber, Rainer Matischek, José Isola, Stefano Cerutti, Claudio Russo et al. "ShapeFuture - Technical Progress After Year 2".	11:30-11:50 Nicolai Lossius Nossum and Amund Skavhaug. "From Assistive Mobility to Active Rehabilitation: A Multi-Stage Evolution of a Cost-Effective Smart Rollator".
12:00-13:30	Lunch Break		
13:30-15:10	**DSD 6-1 | Room A** **European and Major Multi-Partner Projects in Digital Systems Design (EMPDSD), Part 2 of 2** **Chair: TBD**	**DSD 6-2 | Room B** **Sustainable Digital System Design (SDSD)** **Chair: TBD**	
	13:30-13:50 Alkistis Aikaterini Sigourou, Zoya Dyka, Jesus Gutierrez Teran, Peter Langendoerfer, Nicolas Sklavos and Ievgen Kabin. "Preventing Multiplication-Squaring Distinguishability in Cryptographic Hardware".	13:30-13:50 Johannes Knödtel, Maximilian Krentzien, Florian Rokohl and Marc Reichenbach. "Data-Driven Energy Modeling of RISC-V Architectures Using Deep Learning".	
	13:50-14:10 Jiri Gallo, Jan Kastil, Jan Povolny, Simon Zossak, Martin Kostal, Petr Zelinka et al. "Customization of RISC-V Core for Field-Oriented Control Algorithm".	13:50-14:10 Sneha Dandekar, Arun M, Vaishnavi Sharma and Madhav Rao. "Split-Posit Systolic Array Architectures for Resource-efficient Neural Networks".	
	14:10-14:30 George Rafael Gourdoumanis, Maria Pantazi, Ilias Exouzidis, Athanasios Tziouvaras, Tahani Aladwani, Christos Anagnostopoulos et al. "COIN-3D: Towards Cross-Layer Runtime-Aware Reliability Methodologies for Heterogeneous 2.5D/3D Systems".	14:10-14:30 Priyanshu Tyagi, Rhythm Patel, Sparsh Mittal and Rekha Singhal. "AOR-MAC: An Add-Once Reordered MAC Architecture for DSP-Less FPGA Inference".	

	14:30-14:50 Martin Ebetshuber, Norbert Druml, Franz Darrer and Wolfgang Pribyl. "A Platform for Closed-Loop Operation of Piezoelectric 2D MEMS Mirrors".		
	14:50-15:10 Pelopidas Tsoumanis, Georgios-Ioannis Paliaroutis, Dimitris Valiantzas, Nikolaos Sketopoulos, Andreas Tsiougkos, Aristotelis Tsekouras et al. "Fostering Excellence in AI and Semiconductor Innovation in Greece - The Case of HCCC".		
15:15-15:45	Closing Session		